REMARKS

The Office Action dated May 26, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

Claims 1-40 are pending in the present application. Claims 1, 16, and 27 are independent claims. No new matter has been added. Claims 1-40 are respectfully submitted for consideration.

Rejection of Claims 1-2, 6-10, 16-17, 21-24, and 27-29 Under 35 U.S.C. § 103(a):

Claims 1-2, 6-10, 16-17, 21-24, and 27-29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. 2002/0089933 A1 to Giroux et al. (Giroux '933) in view of U.S. Patent No. 6,097,698 to Yang et al. (Yang '698). In the Office Action, it is acknowledged that Giroux '933 fails to disclose determining whether the associated receive port is currently saturated. However, it is alleged in the Office Action that Yang '698 may be combined with Giroux '933 to yield the claimed invention. This rejection is respectfully traversed.

Claim 1, upon which claims 2-15 depend, recites a shared memory packet switching device having a plurality of receive ports for receiving data packets, and a plurality of transmit ports for transmitting data packets. The device recited in claim 1 includes a shared memory providing a shared memory space for temporary storage of data packets received via the receive ports and at least one input logic unit associated with at least one of the receive ports, and being operative to determine whether the

associated receive port is saturated by determining whether a number of packets received via the associated receive port and currently stored in the shared memory exceeds a predetermined drop threshold value. The device also includes a packet routing control unit communicatively coupled with the at least one input logic unit, and being operative to determine a destination one of the transmit ports for each of the received data packets and at least one output logic unit associated with at least one of the transmit ports, the output logic unit being communicatively coupled with the packet routing control unit, and being operative to determine whether the associated transmit port is congested by determining whether a number of packets currently stored in the shared memory that are to be transmitted via the associated transit port exceeds a predetermined congestion threshold value, and also being operative to generate an associated output full signal indicative of whether the associated transmit port is congested. As recited in claim 1, the input logic unit is responsive at least in part to each of the output full signals, and is further operative to cause a selected packet received via the associated receive port to be dropped if the associated receive port is currently saturated and the output full signals indicate that a destination transmit port associated with the selected packet is currently congested.

Claim 16, upon which claims 17-26 depend, recites a shared memory packet switching device having a plurality of receive ports for receiving data packets, and a plurality of transmit ports for transmitting data packets. The device recited in claim 16 includes a shared memory providing a shared memory space for temporary storage of

data packets received via the receive ports, at least one input logic unit associated with at least one of the receive ports, and being operative to determine whether the associated receive port is saturated by determining whether a number of packets received via the associated receive port and currently stored in the shared memory exceeds a predetermined drop threshold value, and a packet routing control unit communicatively coupled with the at least one input logic unit, and being operative to determine a destination one of the transmit ports for each of the received data packets, the packet routing unit being further operative to generate a plurality of transmit signals each being associated with one of the transmit ports, and to assert a particular one of the transmit signals when a received packet is to be transmitted via the associated transmit port. The device also includes at least one output logic unit associated with at least one of the transmit ports, the output logic unit being communicatively coupled with the packet routing control unit, and being operative to determine whether the associated transmit port is congested by determining whether a number of packets currently stored in the shared memory that are to be transmitted via the associated transit port exceeds a predetermined congestion threshold value, and also being operative to generate an associated output full signal indicative of whether the associated transmit port is congested. As recited in claim 16, the packet routing control unit also is responsive to the output fill signals, and is operative to generate a plurality of filter signals for indicating that a received packet is destined for a congested one of the transmit ports. Further, the input logic unit is further responsive to each of the filter signals, and is further operative

to cause a selected packet received via the associated receive port to be dropped if the associated receive port is currently saturated and the filter signals indicate that a destination transmit port associated with the selected packet is currently congested.

Claim 27, upon which claims 28-40 depend, recites a process of controlling the flow of data through a shared memory packet switching device having a plurality of receive ports for receiving data packets, a plurality of transmit ports for transmitting data packets, and a shared memory providing a shared memory space for temporary storage of data packets received via the receive ports. As recited in claim 27, the process includes receiving a packet via an associated one of the receive ports, determining whether the associated receive port is currently saturated by determining whether a number of packets received via the associated receive port and currently stored in the shared memory exceeds a predetermined drop threshold value, and determining a destination one of the transmit ports associated with the received data packet. The process also includes determining whether the destination transmit port is currently congested by determining whether a number of packets currently stored in the shared memory that are to be transmitted via the destination transmit port exceeds a predetermined congestion threshold value and dropping the received packet if the associated receive port is currently saturated and the destination transmit port is currently congested.

As recited in the present specification, among the advantages of the devices and processes according to the claimed invention is that an uncongested transmit port of the device is not starved as a result of flow control functions initiated at a saturated receive

port as a result of heavy traffic through the device between the saturated receive port and a plurality of transmit ports including the uncongested transmit port and other transmit ports, some of which may be congested. It is respectfully submitted that Giroux '933 and Yang '698, taken either individually or in combination, fail to disclose or suggest the elements of any of the presently pending claims. Therefore, it is further submitted that Giroux '933 and Yang '698 fail to provide at least the above-discussed advantages of the claimed invention.

Giroux '933 discloses "an output queuing switch with a shared memory architecture" (Paragraph [0023], lines 1-2). Giroux '933 also discloses "an algorithm that will prevent both the individual output port queues and the aggregate buffer from overflowing, while assuring an acceptable level of fairness to all the contending connections" (Paragraph [0025], lines 3-6).

Yang '698 discloses a "switching node [that] includes...a control element" (Column 2, lines 47-49). Yang '698 also discloses that the "control element discards cells if the cell occupancy of the buffer exceeds a predetermined threshold level and a credit value indicates that the switching node has loaded a number of cells into the buffer for transmission which exceeds a cell loss ratio guarantee provided by the switching node" (Column 2, lines 54-58).

In order to establish a proper case of *prima facie* obviousness, "there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art,...to combine reference teachings"

(M.P.E.P. § 2143). However, as discussed below, Applicants respectfully submit that no such suggestion or motivation exists in either Giroux '933 or Yang '698.

On page 3 of the Office Action, it is alleged that Yang '698 discloses a system that determines if a certain input has exceeded its fair share of the bandwidth. However, Applicants respectfully disagree. In response to this allegation, Applicants point out that "fairness" is neither disclosed nor suggested in Yang '698. Rather, the guarantees disclosed in Yang '698 are inherently "unfair" because they, by design, allow for certain inputs to use up a greater portion of a buffer than others. Therefore, at least since Yang '698 fails to disclose or suggest the concept of fairness, Applicants respectfully submit that one of skill in the art would not be motivated to combine Yang '698 and Giroux '933 and that no proper *prima facie* case of obviousness can be made using these two references.

Also on page 3 of the Office Action, it is further alleged that one of skill in the art would have been motivated to combine Giroux '933 and Yang '698 to ensure that a certain input doesn't dominate the input and take over too much space in the buffer. Again, Applicants respectfully disagree. In response to this further allegation, Applicants respectfully submit that Yang '698 not only fails to disclose or suggest a mechanism for preventing a certain input from taking over too much space in the buffer, but actually provides a method for allowing an input to take over a disproportionate share the entire buffer.

More specifically, Yang '698 allows for one buffer input to be given a very high guarantee and for all other buffer inputs to be given very low guarantees. In such a situation, one input would be allowed to dominate the use of practically the entire buffer, while all other inputs would be allowed only very limited use of the buffer. Since such a situation is precisely what Giroux '933 attempts to prevent, Applicants again respectfully submit that one of skill in the art would not be motivated to combine Giroux '933 and Yang '698 and that a proper case of *prima facie* obviousness cannot be made using these two references.

In addition to the above, Applicants respectfully submit that Giroux '933 and Yang '698, taken either individually or in combination, fail to disclose or suggest at least the "at least one input logic unit" recited in claims 1-26 of the present application, "being further operative to cause a selected packet...to be dropped if said associated receive port is currently saturated". Also, Applicants respectfully submit that Giroux '933 and Yang '698, taken either individually or in combination, fail to disclose or suggest at least "dropping said received packet if said associated receive port is currently saturated", as recited in claims 27-40.

On page 7 of the outstanding Office Action, it is alleged that the buffer illustrated in Figure 4 of Yang '698 is connected to the VCn inputs and can therefore be considered an input buffer. On the same page of the Office Action, it is further alleged that Yang '698 discloses that when the cell occupancy of the buffer exceeds a predetermined threshold level associated with a particular VCn, control element 35 can discard a cell

received by the switching mode associated with the VCn. Based on these allegations, it is further alleged on page 7 of the Office Action that Yang '698 discloses dropping packets when an input threshold has been exceeded. Applicants yet again disagree.

In response to the above allegations, Applicants first respectfully point out that the VCns disclosed in Yang '698 are not analogous to the "receive ports" recited in claims 1-40 of the present application. Rather, at best, the "receive ports" recited in the claimed invention may be, in some ways, analogous to the "input communication links 13(p)(i)" disclosed in Yang '698. As such, since Yang '698 discloses in Figure 3 thereof that links 13(p)(i) are connected to input interface 30 and further discloses, on lines 33-36 of column 6 thereof, that input interface 30 provide cells for the VCns, one of skill in the art would understand that VCn and receive ports differ significantly from each other.

Based on the above, even if it is assumed, *arguendo*, that control element 35 can indeed discard a cell received by the switching mode associated with the VCn, Giroux '933 and Yang '698, taken either individually or in combination, still fail to disclose or suggest the claimed invention.

At least in view of the above remarks, reconsideration and withdrawal of the rejection of claims 1-2, 6-10, 16-17, 21-24, and 27-29 under 35 U.S.C. § 103(a) as being unpatentable over Giroux '933 in view of Yang '698 is respectfully requested.

Rejection of Claims 30-31 and 33-35 Under 35 U.S.C. § 103(a):

Claims 30-31 and 33-35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Giroux '933 in view of Yang '698, further in view of U.S. Patent No. 5,78,071 to Basso et al. (Basso '071) and in light of the rejection of claim 27. In the Office Action, it is acknowledged that neither Giroux '933 nor Yang '698 discloses asserting a backpressure signal when a backpressure threshold has been exceeded. However, it is alleged in the Office Action that Basso '071 may be combined with Giroux '933 and Yang '698 to yield the claimed invention. This rejection is respectfully traversed.

As previously discussed, Giroux '933 discloses an algorithm based on fairness to manage the buffer disclosed therein while Yang '698 uses guarantees to manage the buffer disclosed therein. As also previously discusses, one of skill in the art would therefore not be motivated to combine Giroux '933 and Yang '698.

Basso '071 discloses "a data traffic control system which can be fair and loss-free even with small buffer capacity" (Column 2, lines 35-36). Basso '071 also discloses that "[e]ach node has a buffer for storing a queue for each NRB connection" (column 2, lines 51-52).

However, Basso '071 fails to address or eliminate any of the shortcomings of Giroux '933 and Yang '698. Therefore, Applicants respectfully submit that Giroux '933 and Yang '698, even in view of Basso '071, are still not properly combinable and that the rejection of claims 30-31 and 33-35 is therefore improper at least for this reason.

At least in view of the above remarks, reconsideration and withdrawal of the rejection of claims 30-31 and 33-35 under 35 U.S.C. § 103(a) as being unpatentable over Giroux '933 in view of Yang '698, further in view of Basso '071 and in light of the rejection of claim 27 is respectfully requested.

Allowable Subject Matter:

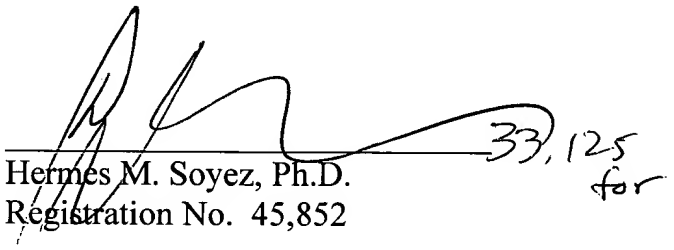
Applicants thank the Examiner for acknowledging that claims 3-5, 11-15, 18-20, 25-26, 32, and 36-40 contain allowable subject matter. At least in view of the above remarks, Applicants respectfully submit that claims 3-5, 11-15, 18-20, 25-26, 32, and 36-40 are in allowable form.

Applicants respectfully submit that all of the comments included in the Office Action have been addressed and that the rejections included therein have been overcome. Hence, Applicants respectfully further submit that claims 1-40 contain allowable subject matter. Therefore, it is respectfully requested that all claims pending in the present application be allowed, and that this application be passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned representative at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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